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# Design of an Efficient Arithmetic Logic Unit using Quantum Dot Cellular Automata

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**Abstract**

There is a new nano-scale technology called Quantum-dot Cellular Automata (QCA) that has the potential to replace CMOS technology since it greatly improves the design of electronic circuits. In order to do the logical and arithmetic operations that the multiplexer and full adder are crucial to, the Arithmetic Logic Unit (ALU) is an essential part of the Central Processing Unit (CPU). Based on the concept of cell interaction with a reduced cell count, this research proposes a QCA multiplexer. In a similar vein, a QCA multilayer ALU may execute logical and mathematical operations. Implementations of both 1 bit and 4 bit ALUs are shown in this work. The results of the simulation are run and validated using the QCAD programme. The simulation results show that the suggested structures are more efficient and use less power than the current ALU.

**Keywords:** The acronyms QCA, CPU, ALU, multiplexer, and full adder stand for quantum-dot cellular automata.

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## INTRODUCTION

Current Very Large Scale Integration (VLSI) circuits are typically designed using CMOS, a well-known technology. However, CMOS has a number of limitations, including physical, material, power-thermal, technological, and economic ones. To address these limitations, a new technology called QCA has emerged. This technology is a viable substitute for transistor-based technology because of its unique requirements, which include very low power consumption, high component density, and incredibly tiny feature size at the molecular or even atomic level [1]. A nano-scale square containing two mobile electrons and four charged containers called quantum dots in each corner makes up a QCA cell, the fundamental component of this technology. In addition to switching the occupancy of the two electrons, a single QCA cell may only accept two fully polarised states, referred to as cell polarisation (p = +1, p = -1). When compared to traditional CMOS circuits, QCA calculations use much less power because they do not involve any electrical current. Most QCA systems use the four-zone design, also called Landauer clocking, which consists of the Relax, Switch, Hold, and Release stages [2]. Furthermore, there are a number of methods for crossing wires on top of each other, including logical crossing, multilayer crossing, and single-layer crossing [2].
Based on the explicit interactions between QCA cells, this research proposes a novel application-specific QCA 2:1 multiplexer. In addition, a novel QCA full adder is suggested to improve the associated operations based on the data derived from ALU's mathematical operations, taking into account that the majority of ALU's mathematical operations may be executed using the sum operation.
In order to reduce the number of cells, a new multilayer 1-bit ALU is constructed using the suggested complete adder with minor changes to the existing ALU. The suggested buildings are also compared to the comparable designs in terms of their energy efficiency and structural soundness.

Here is how the remainder of this paper is structured: In Section III, the relevant literature

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is detailed.This paper's approach is covered in Section IV. The outcomes of the suggested procedure are examined in SECTION V. Section VI brings this study to a close.

## I. RELATED WORKS

An ALU can carry out basic arithmetic operations such as sum, subtraction, multiplication, and division, also, bitwise logical operations such as NOT, AND, and OR on integer binary numbers. Typically, binary information in computers is represented in 16-, 32- and 64-bit quantities. However, to make our design, we have concentrated our design concepts in present work on using 1-bit quantities. The 16-, 32- and 64-bit ALU can be designed in the same manner. The logical diagram of the existed 1-bit ALU circuit as shown in Figure 1

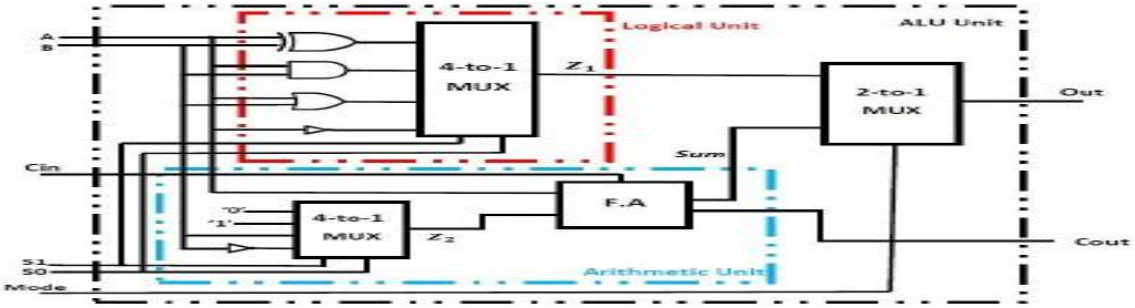


Figure.1: Logical diagram of 1-bit ALU

The logical diagram and multilayer QCA layout of the full adder circuit are shown in Figure 2 and Figure 3, respectively. Generally, Full Adder (FA) is one of the most frequently utilized components in the arithmetic operations [17]. This block in addition to the sum operation can be applied in other arithmetic operations such as multiplication, division, and subtraction. The FA is a three-input digital circuit that calculates the sum of the two digits (*A* and *B*) as operands and one bit (*Cin*) as quoting from the previous adder; also, produces two outputs i.e., *Sum*

(S) and *Carry Out* (Cout). In a full adder, the *Carry Out* and *Sum* can be calculated by Eqn. 1 and Eqn. 2, respectively.

$CarryOut=ab+ac+bc=M(a,b,c)$-------- (1)

$Sum=a\oplus b\oplus c$ ---------- (2)

Where *M*, represents the majority gate.

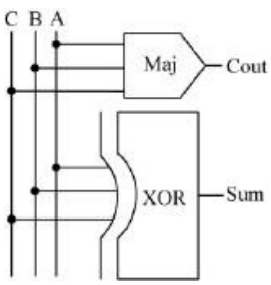


Figure 2:Logic diagram of full adder structure

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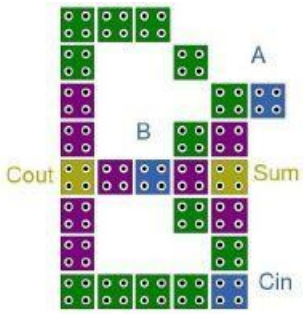
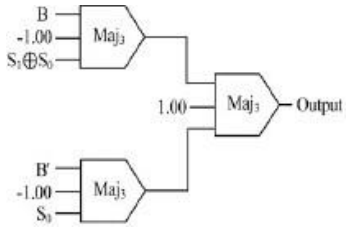
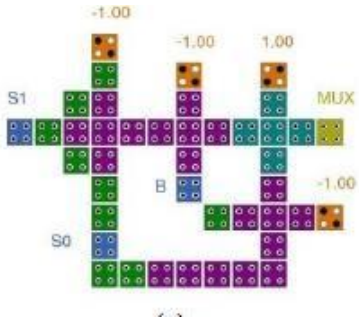



Figure 3:QCA layout of full adder structure

The logical diagram and its layout of the QCA 4:1 multiplexer are shown in Figure. 4




(a)




(b)

Figure. 4: (a) Logical diagram (b) QCA layout, of the application-specific QCA 4:1 multiplexer.

## METHODOLOGY

To perform arithmetic operation 4:1 multiplexer is removed and replaced with ex-or gate in order to decrease the cell count, designs with and without 4:1 Mux at the Arithmetic Block are implemented in this work, the proposed ALU 1-bit is implemented in 5 layers in order to decrease the cell count & its Qca layout is shown in Figure 5. Table 1 shows the basic operation s. Mode 0 selects logical operation Mode 1 selects Arithmetic operations, only S0 will be the select line for 2:1 Mux which has replaced 4:1 Mux at the Arithmetic block. Input to 2:1 is B and ~B, thus a XOR gate with input as B and S0 will suffice the need.Table 2: Basic operations controls

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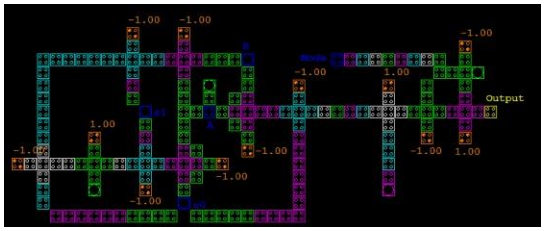
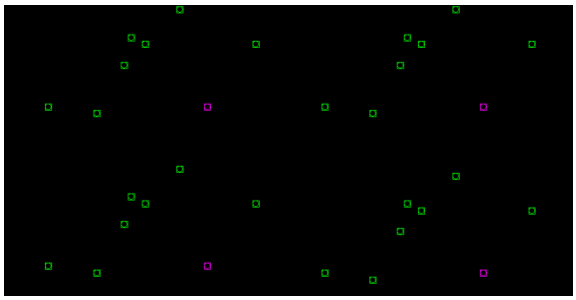
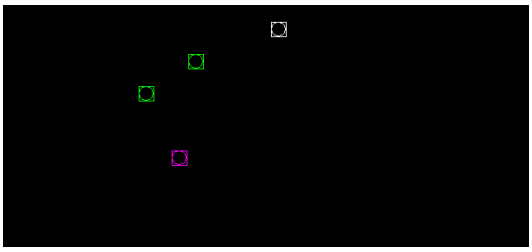
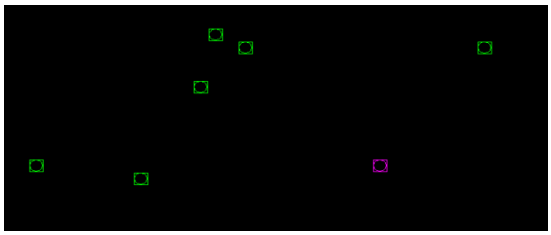
| Mode | S1 S0 | Operation |
|---|---|---|
| 0 | 0 0 | A XOR B |
| 0 | 0 1 | A AND B |
| 0 | 1 0 | A OR B |
| 0 | 1 1 | ~A |
| 1 | _ 0 | A+B+Cin |
| 1 | _ 1 | A+~B+Cin |



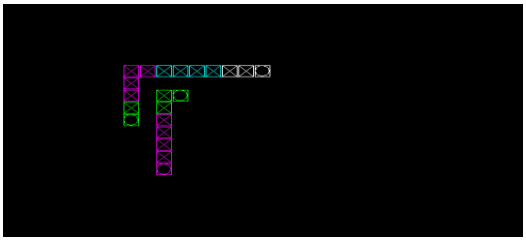







(a)

(b)



(a) layer 1

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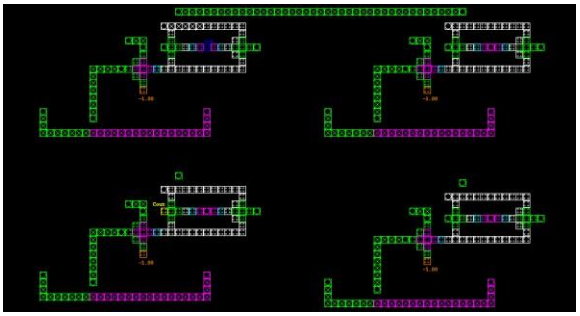
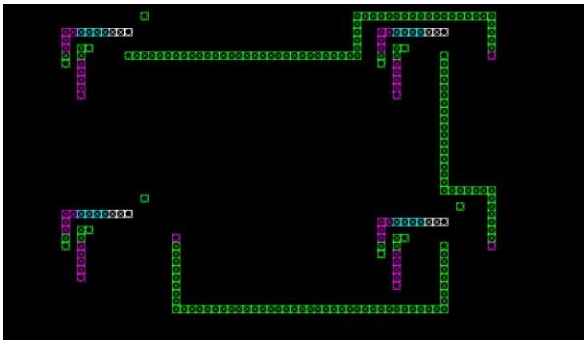
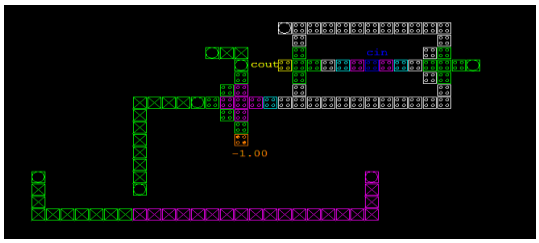
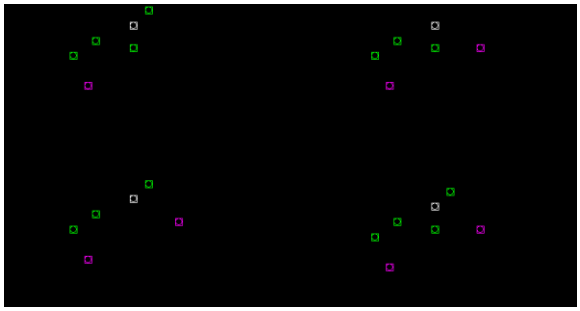


## II. RESULTS &DISCUSSIONS





Therefore, in this research, we present a 1-bit and 4-bit ALU with a suggested multiplexer; these ALUs have much less power consumption and space than the current design, as well as when compared to the traditional CMOSALU. The ALUs that are suggested are created and put into action using the QCAD software.
Fig. 7(b), the The outcome of the 1-bit ALU simulation The simulations of a complete adder, with inputs a, b, and c and outputs total and carry, are shown in Figure 7(a). The simulation results of the one-bit ALU are shown in Figure 7(b). The inputs to the ALU are a, b, c, s0, and s1, and the mode parameter determines whether the ALU should execute arithmetic or logical operations. The outputs of the ALU are out and cout.

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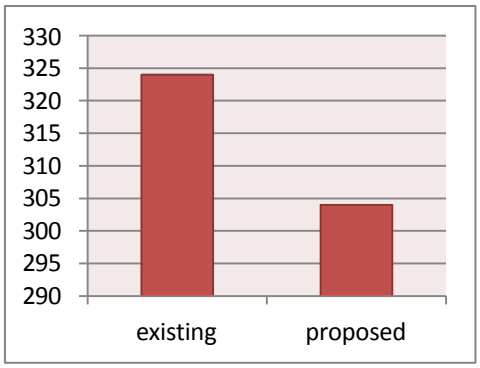


Figure 8: Area(cell count) Comparison between the proposed 1-bit ALU with existing 1-bit ALU

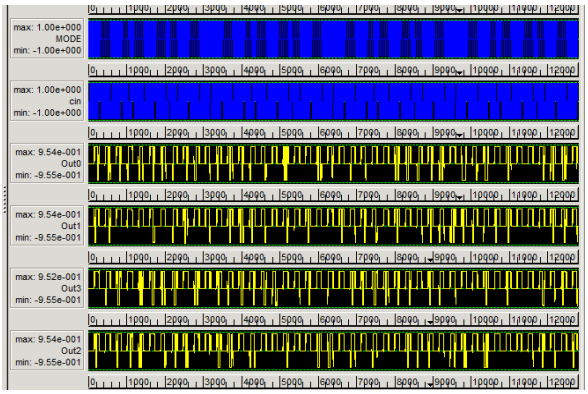


Figure 9: Simulation results of 4-bit ALU

Further Table 2 shows the comparison of power Energy dissipation of ALU design in CMOS and QCA , Table 3 shows the further improvement in the design in terms of Number of cells and Energy which is achieved by replacing 4:1 Mux in Arithmetic block with a xor gate, which is nothing but a 2:1 Mux with B and ~B as inputs.

Table 2: Energy comparison

| Design | Energy |
|---|---|
| 1bit ALU in CMOS | 5.16 pJ |
| 1bit ALU in QCA | 20.16 zJ (0.126eV) |
| 4 bit ALU in CMOS | 17.45 pJ |
| 4 bit ALU in QCA | 85.7 zJ (0.536eV) |

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Table 3: No of Cells and Energy comparison

| Design | No of Cells | Energy(zJ) |
|---|---|---|
| 1 bit ALU with 4:1 Mux at Arithmetic block | 324 | 20.16 |
| 4 bit ALU with 4:1 Mux at Arithmetic block | 1365 | 85.72 |
| 1 bit ALU with xor at Arithmetic block | 304 | 18.72 |
| 4 bit ALU with xor at Arithmetic block | 1333 | 82.91 |

## III. CONCLUSION

The study suggests a new multilayer QCA ALU architecture that can do mathematical and logical operations on bits. In addition, a simpler ALU with a more efficient multiplexer option for the arithmetic block has been proposed, which uses less cells than the previous design. So, you may make ALU designs with either one or four bits using the QCAD tool. In comparison to existing methods, the results show that the proposed structure for 1-bit QCA ALU uses less power and uses fewer cells. This study also examines and suggests a 4-bit ALU for use in QCA.

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